



Intel® Wireless Flash Memory (W18 SCSP)

32-Mbit W18 + 8-Mbit SRAM (38F1020W0YTQ0, 38F1020W0YBQ0)

Datasheet

Product Features

- **Flash Architecture**
 - Flexible, Multi-Partition, Dual-Operation: Read-While-Write / Read-While-Erase
 - 8 Partitions, 4 Mbits each
 - 7 Main Partitions, 8 Main Blocks each
 - 1 Parameter Partition, 8 Parameter + 7 Main Blocks
 - 32-KWord Main Blocks, 4-KWord Parameter Blocks
 - Top and Bottom Parameter Configuration
- **Flash Performance**
 - 65 ns Initial Access Speed
 - 25 ns Page-Mode Read Speed; 4-Word Page
 - 14 ns Burst-Mode Read Speed
 - 4-, 8-, 16- or Continuous-Word Burst Modes
 - Burst- and Page-Mode Reads in Parameter and Main Partitions
 - Burst Suspend
 - Burst-Mode Reads can Traverse Partition Boundaries
 - Programmable WAIT Polarity
 - Enhanced Factory Programming: 3.1 μ s/Word (typ)
- **Flash Data Protection**
 - Absolute Protection with VPP and WP#
 - Individual Dynamic Zero-Latency Block Locking
 - Individual Block Lock-Down
 - Erase/Program Lockout during Power Transitions
- **Flash Protection Register**
 - 64 Unique Device Identifier Bits
 - 64 User-Programmable OTP Bits
- **Flash Automation Suspend Operations**
 - Erase Suspend to Program or Read
 - Program Suspend to Read
 - 5 μ s (typ) Program/Erase Suspend Latency
- **Flash Software**
 - Intel® Flash Data Integrator (Intel® FDI) Optimized
 - Common Flash Interface (CFI)
- **SCSP Architecture**
 - 32-Mbit Flash die + 8-Mbit SRAM die
 - Reduces Board Space Requirement
 - Simplifies PCB Design Complexity
 - Easy Migration to Future SCSP Devices
- **SCSP Voltage**
 - 1.7 V to 1.95 V V_{CC}/V_{CCQ} and S- V_{CC}
- **SCSP Packaging**
 - 0.8 mm Ball-Pitch Intel® SCSP
 - Area: 8x10 mm, Height: 1.2 mm max
 - 88-Ball (8 x 10 Matrix): 80 Active Balls with 2 Support Balls at Each Corner
- **SRAM Architecture and Performance**
 - 70 ns Access Time
 - Low-Voltage Data Retention Mode
- **Flash Quality and Reliability**
 - Extended Temperature: -25 °C to +85 °C
 - Minimum 100,000 Block Erase Cycles
 - Intel® 0.13 μ m ETOX™ VIII Process Technology

By stacking the Intel® Wireless Flash Memory (W18) device in combination with a low-power 8-Mbit SRAM device, a versatile and compact Stacked Chip Scale Package (SCSP) provides a solution for high-performance, low-power, board-constrained memory applications. This datasheet describes the key features of this 32-Mbit W18 + 8-Mbit SRAM combination device. Refer to the latest revision of the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) for flash device details not provided in this document.

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Revision History

Date of Revision	Version	Description
2/12/03	-001	Original SCSP release.
9/03	-002	Added number column to flash and RAM AC tables and updated title.
5/04	-002	Reformatted the datasheet according to the new layout.

1.0 Introduction

This document contains information pertaining to the Intel[®] Wireless Flash Memory (W18 SCSP); 32-Mbit W18 + 8-Mbit SRAM SCSP device (38F1020W0YTQ0 and 38F1020W0YBQ0). The intent of this datasheet is to provide information about this SCSP device where it may differ from the discrete Intel[®] Wireless Flash memory (W18) device. Refer to the *Intel[®] Wireless Flash Memory (W18) Datasheet* (order number 290701) for information not provided by this document.

1.1 Nomenclature

0x	Hexadecimal prefix
k	1000
M	1,000,000
Byte	8 bits
Word	16 bits
Kword	1024 words
Mbits	1,048,576 bits
SCSP	Stacked Chip Scale Package

1.2 Conventions

Device: Term used interchangeably throughout this document to denote either a particular die or both die in the package.

VCC or VPP vs. V_{CC} or V_{PP}: When the reference is to signal or package connection name, the notation will be VCC or VPP. When the reference is to timing or level, the notation will be subscripted (e.g., V_{CC} or V_{PP}).

R-OE#, R-LB#, R-UB#, R-WE#: Used to identify OE#, LB#, UB#, WE#, RAM signals.

2.0 Functional Overview

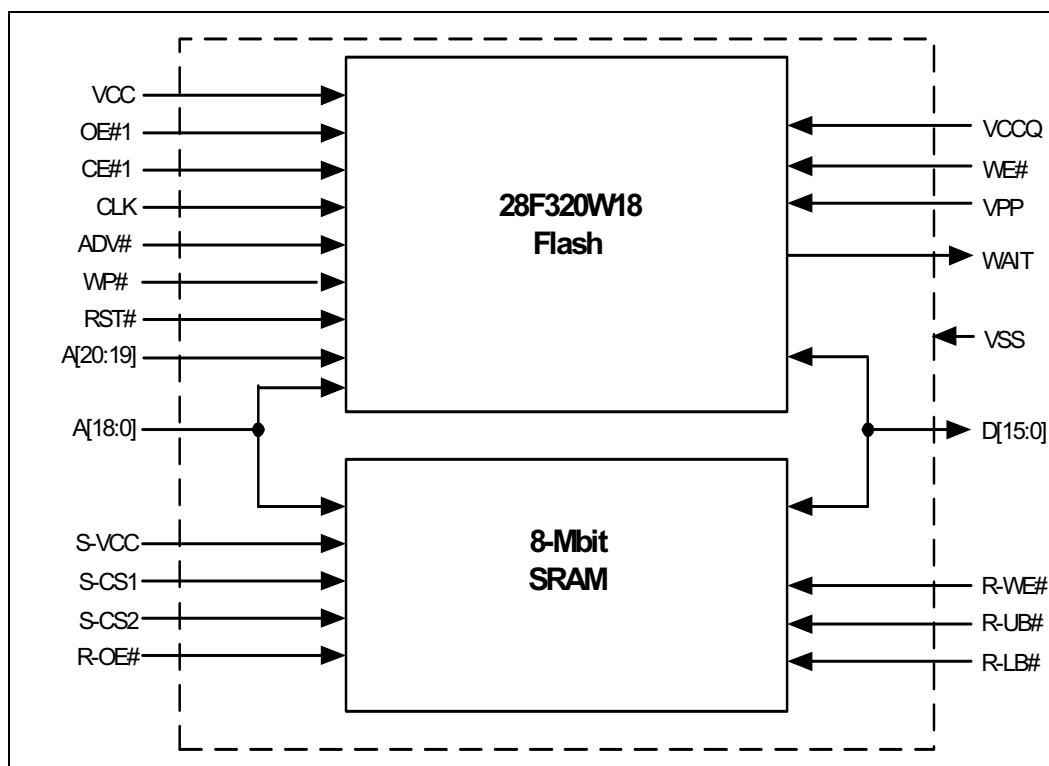
This section provides an overview of the features of the 38F1020W0YTQ0 and 38F1020W0YBQ0 devices.

The 38F1020W0YTQ0 and 38F1020W0YBQ0 devices combine one flash and one SRAM die into a single package. Please refer to the discrete W18 datasheet for a complete overview of the flash product features.

2.1 Block Diagram

Figure 1 contains the block diagram of the 38F1020W0YTQ0 and 38F1020W0YBQ0 devices. Refer to Table 1, “Signal Descriptions” on page 10 for a description of each signal shown.

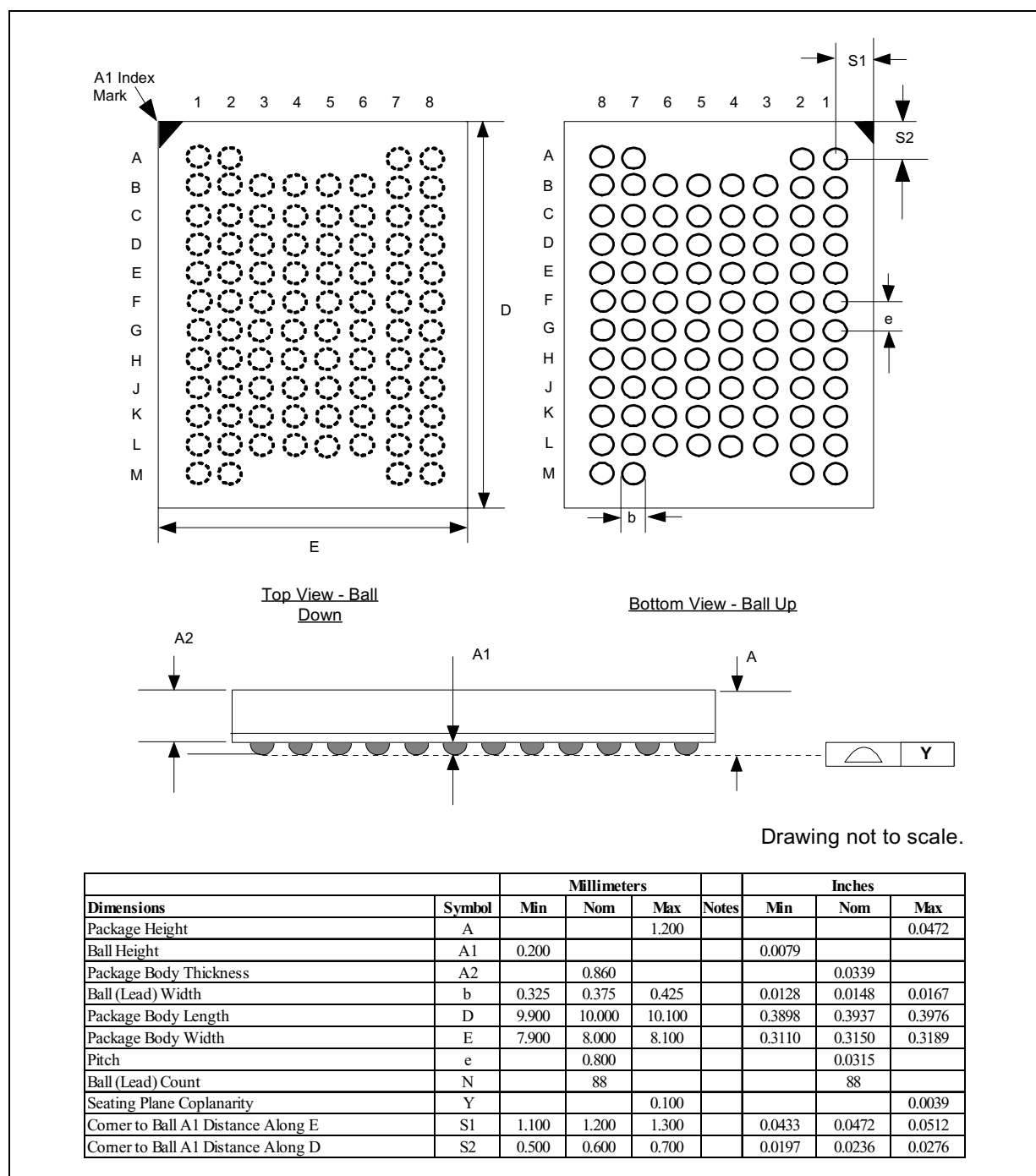
Figure 1. Block Diagram



3.0 Package Information

3.1 88-Ball Mechanical Specification

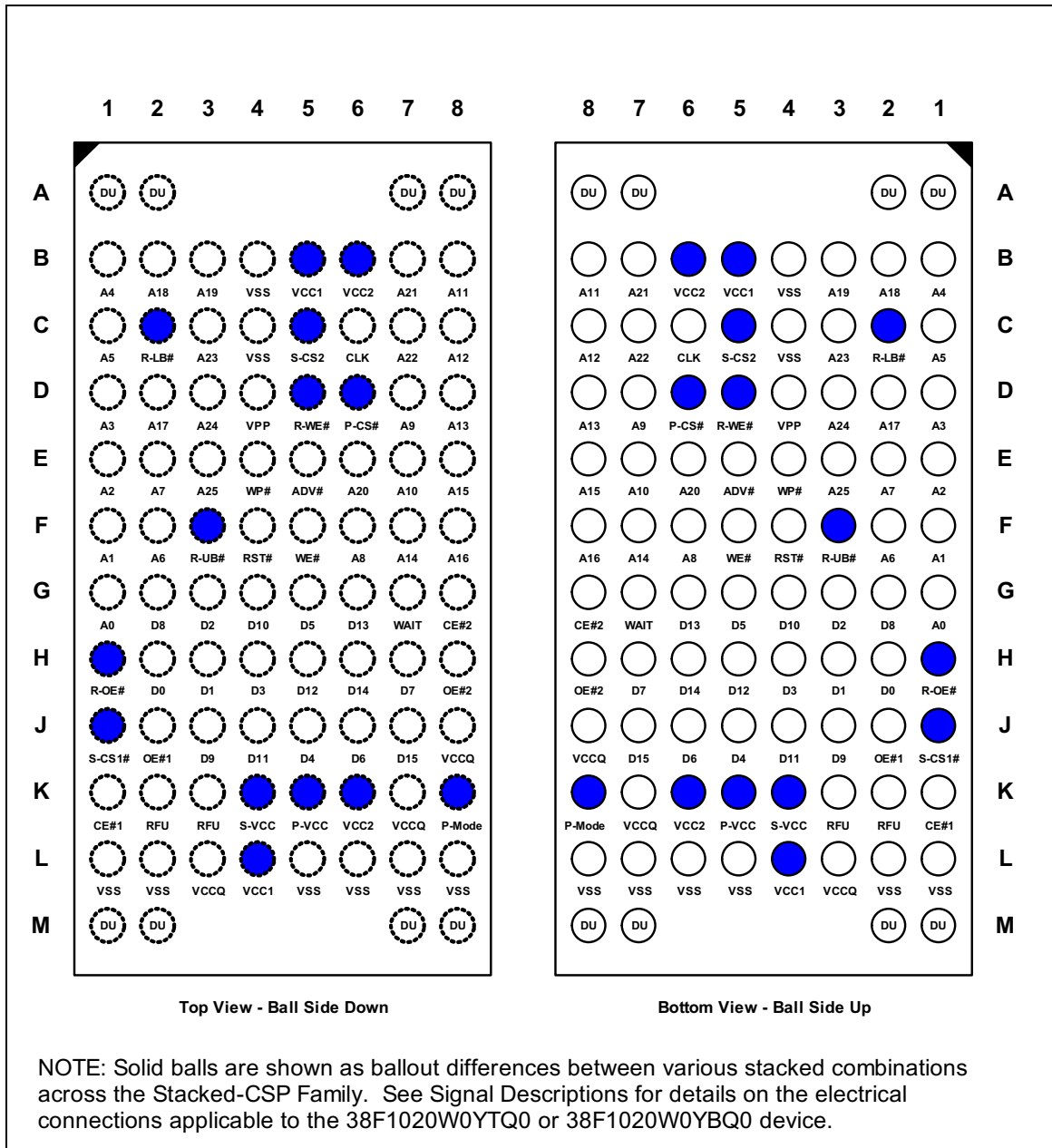
Figure 2. 88-Ball Mechanical Specification



4.0 Ballout and Signal Description

The 38F1020W0YTQ0 and 38F1020W0YBQ0 devices are available in an 88-ball SCSP with ball pitch of 0.8 mm. Figure 3 contains the ballout.

Figure 3. 88-Ball SCSP Package Diagram



4.1 Signal Descriptions

Table 1 describes the active signals used on the 38F1020W0YTQ0 and 38F1020W0YBQ0 devices.

Table 1. Signal Descriptions (Sheet 1 of 2)

Symbol	Type	Name and Function
A[25:0]	Input	<p>ADDRESS INPUTS: Decodes a specific location for reads or writes, or targets a Flash block for erase. Flash addresses are latched during writes, and for reads when ADV# (or CLK with ADV# low) is issued.</p> <p>A[20:0] decodes a specific location within the 28F320W18 die.</p> <p>A[18:0] decodes a specific location within the 8-Mbit SRAM.</p> <p>A[25:21] is not used in this device and may be treated as RFU.</p>
D[15:0]	Input/ Output	<p>DATA INPUTS/OUTPUTS: Inputs data for SRAM writes or Flash programming. Flash commands issued during CUI writes are input on D[7:0] only.</p> <p>D[15:0] outputs device memory contents or Flash ID codes. Flash SRD is read on D[7:0] only. D[15:0] are floated when the device is deselected or the outputs are disabled. Flash I/Os D[15:8, 6:0] are floated when the Flash WSM is busy.</p>
CE#1, CE#2	Input	<p>FLASH CHIP ENABLE: CE#1-low selects the Flash component. When asserted, the Flash internal control logic, input buffers, decoders, and sense amplifiers are activated. When deasserted, the Flash die is deselected, power levels reduce to standby, and data and WAIT outputs are placed in high-Z state.</p> <p>CE#2 is not used in this device and may be treated as RFU.</p>
S-CS1#, S-CS2	Input	<p>SRAM CHIP SELECTS: Activates the SRAM internal control logic, input buffers, decoders, and sense amplifiers. When either are deasserted (S-CS1# = V_{IH} or S-CS2 = V_{IL}), the SRAM is deselected and its power reduces to standby levels.</p>
RST#	Input	<p>FLASH RESET: RST#-low resets Flash internal circuitry and inhibits write operations. This function may be employed to provide data protection during power transitions. After exiting the reset state (RST# returned to logic-high), the selected Flash die resumes operation in asynchronous read-array mode.</p>
OE#1, OE#2	Input	<p>FLASH OUTPUT ENABLE: OE#1-low activates device output through the Flash data buffers during a Flash read cycle. When deasserted, the Flash outputs tri-state to high-Z.</p> <p>OE#2 is not used in this device and may be treated as RFU.</p>
R-OE#	Input	<p>SRAM OUTPUT ENABLE: R-OE#-low activates device output through the SRAM data buffers during a SRAM read cycle. When deasserted, the SRAM outputs tri-state to high-Z.</p>
WE#	Input	<p>FLASH WRITE ENABLE: WE# controls writes to the selected Flash die. WE#-low allows input to the Flash CUI, array, PR/PLR, RCR, or block lock bits. Addresses and data are latched on this signal's rising edge.</p>
R-WE#	Input	<p>SRAM WRITE ENABLE: R-WE#-low allows writes to the SRAM array.</p>
R-UB#, R-LB#	Input	<p>SRAM UPPER / LOWER BYTE ENABLES: R-UB#-low enables the SRAM high-order bytes (D[15:8]). R-LB#-low enables the SRAM low-order bytes (D[7:0]).</p>
ADV#	Input	<p>FLASH ADDRESS VALID: During synchronous reads, Flash addresses are latched on the ADV# rising edge or on a CLK transition with ADV# low. For asynchronous reads, ADV# can be driven high to latch an address or it can be held low throughout the read cycle.</p>
CLK	Input	<p>FLASH CLOCK: CLK synchronizes the Flash device to the system bus frequency. Used only for burst reads, CLK increments the internal address generator within the Flash device. Externally-applied addresses are latched by the Flash device via a CLK transition if ADV# is asserted low.</p>
WAIT	Output	<p>FLASH WAIT: Indicates that Flash D_{OUT} is not yet valid. Used only for synchronous reads. WAIT is high-Z whenever CE#1 is deasserted, but is not gated by OE#1.</p>

Table 1. Signal Descriptions (Sheet 2 of 2)

Symbol	Type	Name and Function
WP#	Input	FLASH WRITE PROTECT: Enables/disables the Flash lock-down mechanism. WP#-low secures locked-down blocks from software unlock attempts. WP#-high overrides the lock-down function, thus allowing system software to unlock locked-down blocks.
VPP	Power	FLASH PROGRAM/ERASE SUPPLY: Hardware program and erase protection. A valid voltage level allows program or erase; memory contents cannot be altered when V_{PP} is at or below the V_{PP} lockout voltage (V_{PPLK}). Program or erase at invalid V_{PP} voltages should not be attempted. Set $V_{PP} = V_{CC}$ for in-system read, program and erase operations. V_{PP} must remain above V_{PP1MIN} for in-system program or erase operations. V_{PP2} can be applied to main blocks for 1000 cycles maximum and to parameter blocks for 2500 cycles. V_{PP} can be V_{PP2} for cumulative total, not to exceed 80 hours maximum. Extended use of V_{PP} at V_{PP2} may reduce block cycling capability.
VCC	Power	FLASH POWER SUPPLY: Supplies power to the Flash core.
S-VCC	Power	SRAM POWER SUPPLY: Supplies power for SRAM operations.
VSS	Power	GROUND: Do not float any VSS connection.
RFU	—	RESERVED for FUTURE USE: RFU locations are NC (no connect) on this product. Contact Intel regarding their future use.
DU	—	DO NOT USE: Do not drive, leave disconnected.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Absolute maximum ratings for the 38F1020W0YTQ0 and 38F1020W0YBQ0 devices are shown in Table 2.

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

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Table 2. Absolute Maximum Ratings

Parameter	Maximum Ratings		Unit	Notes
	Min	Max		
Temperature under Bias Expanded	-25	+85	°C	
Storage Temperature	-65	+125	°C	
Voltage On Any Signal (except V_{CC} , V_{CCQ} , V_{PP} and $S-V_{CC}$)	-0.5	+2.45	V	1
V_{CC} Voltage	-0.2	+2.45	V	1
V_{CCQ} and $S-V_{CC}$ Voltage	-0.2	+2.45	V	1
V_{PP} Voltage	-0.2	+14	V	1,2
Output Short Circuit Current	-	100	mA	3

NOTES:

- Specified voltages are with respect to V_{SS} . Minimum DC voltage is -0.5 V on inputs and I/Os, and -0.2 V on V_{CC} , V_{CCQ} , V_{PP} and $S-V_{CC}$ supplies. During transitions, this level may undershoot to -2.0 V for periods < 20 ns. During transitions, the maximum DC voltage level may overshoot to V_{CC} + 2.0 V for periods < 20 ns.
- V_{PP} program voltage is normally V_{PP1} . Maximum DC voltage on V_{PP} may overshoot to +14 V for periods < 20 ns. V_{PP} can be V_{PP2} for 1000 erase cycles on main blocks, 2500 cycles on parameter blocks.
- Output shorted for no more than one second. No more than one output shorted at a time.

5.2 Operating Conditions

Table 3. Temperature and Voltage Operating Conditions

Symbol	Parameter	Min	Max	Unit	Test Condition
T_A	Operating Temperature	-25	+85	°C	Ambient Temperature
V_{CC}	Flash Supply Voltage	1.7	1.95	V	
V_{CCQ}	Flash I/O Voltage	1.7	1.95	V	
V_{PP1}	Flash Program Logic Level	0.9	1.95	V	
V_{PP2}	Flash Factory Program Voltage	11.4	12.6	V	
$S-V_{CC}$	SRAM Supply Voltage	1.7	1.95	V	

5.3 Capacitance

Table 4. Capacitance

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance, Flash (CE#1, OE#1, WE#, RST#, WP#, ADV#, CLK, A[20:19])	6	8	pF	$V_{IN} = 0.0\text{ V}$
C_{IN}	Input Capacitance, SRAM (S-CS#1, S-CS2, R-OE#, R-WE#, R-UB#, R- LB#)	10	10	pF	$V_{IN} = 0.0\text{ V}$
C_{IN}	Input Capacitance, Flash and SRAM (A[18:0])	16	18	pF	$V_{IN} = 0.0\text{ V}$
C_{OUT}	Output Capacitance, Flash and SRAM (D[15:0])	18	22	pF	$V_{OUT} = 0.0\text{ V}$
C_{OUT}	Output Capacitance, Flash (WAIT)	8	12	pF	$V_{OUT} = 0.0\text{ V}$

NOTE: Sampled, not 100% tested. $T_A = +25\text{ °C}$, $f = 1\text{ MHz}$.

6.0 Electrical Specifications

6.1 DC Characteristics

Refer to the discrete *W18 Datasheet* for flash DC current parameters and DC voltage information.

Table 5. SRAM DC Characteristics

Parameter	Description	Test Conditions	1.8 V SRAM		Unit
			Min	Max	
V_{CC}	Voltage Range		1.7	1.95	V
V_{DR}	V_{CC} for Data Retention		1.0	–	V
I_{CC}	Operating Current at min cycle time	$I_{IO} = 0$ mA	–	35	mA
I_{CC2}	Operating Current at max cycle time (1us)	$I_{IO} = 0$ mA	–	6	mA
I_{SB}	Standby Current	S-CS1#>= S- $V_{CC}-0.2V$ or S-CS2<= $V_{SS}+0.2V$ Address/Data toggling at minimum cycle time	–	20	μA
I_{DR}	Current in Data Retention mode	1.8 V SRAM: S- $V_{CC} = 1.0$ V	–	10	μA
V_{OH}	Output HIGH Voltage	$I_{OH} = -100\mu A$	S- $V_{CC}-0.15$	–	V
V_{OL}	Output LOW Voltage	$I_{OL} = 100\mu A,$ V_{CCMIN}	-0.1	0.2	V
V_{IH}	Input HIGH Voltage		S- $V_{CC}-0.4$	S- $V_{CC}+0.2$	V
V_{IL}	Input LOW Voltage		-0.2	0.4	V
I_{OH}	Output HIGH Current		–	–	mA
I_{OL}	Output LOW Current		–	–	mA
$*I_{IL}$	Input Leakage Current	$-0.2 < V_{in} < S-V_{CC} + 0.2$ V	-1	+1	μA
$*I_{LDR}$	Input Leakage Current in Data Retention Mode	$-0.2 < V_{in} < S-V_{CC} + 0.2$ V S- $V_{CC} = V_{DR}$	-1	+1	μA

* Input leakage currents include Hi-Z output leakage for bi-directional buffers with tri-state outputs.

7.0 AC Characteristics

7.1 Flash AC Characteristics

Refer to the *Intel® Wireless Flash Memory (W18) Datasheet* (order number 290701) for flash AC characteristics details not included in [Table 6](#) below.

Table 6. Flash AC Read Characteristics

Number	Sym	Parameter	W18		Unit
			Min	Max	
Asynchronous Specifications					
R1	t_{AVAV}	Read Cycle Time	65		ns
R2	t_{AVQV}	Address to Output Delay		65	ns
R3	t_{ELQV}	CE# Low to Output Delay		65	ns
Latching Specifications					
R108	t_{APA}	Page Address Access Time		25	ns

7.2 SRAM AC Characteristics

Table 7. SRAM AC Characteristics—Read Operations

Number	Symbol	Parameter	Min	Max	Unit	Notes
R1	t_{RC}	Read Cycle Time	70	–	ns	
R2	t_{AA}	Address to Output Delay	–	70	ns	
R3	t_{CO1}	S-CS1# to Output Delay	–	70	ns	
R3	t_{CO2}	S-CS2 to Output Delay	–	70	ns	
R4	t_{OE}	R-OE# to Output Delay	–	35	ns	
R5	t_{BA}	R-UB#, R-LB# to Output Delay	–	70	ns	
R6	t_{LZ}	S-CS1# or S-CS2 to Output in Low-Z	5	–	ns	1,2
R7	t_{OLZ}	R-OE# to Output in Low-Z	0	–	ns	1
R8	t_{HZ}	S-CS1# or S-CS2 to Output in High-Z	0	25	ns	1,2,3
R9	t_{OHZ}	R-OE# to Output in High-Z	0	25	ns	1,3
R10	t_{OH}	Output Hold (from Address, S-CS1#, S-CS2, or R-OE# Change, whichever Occurs First)	0	–	ns	

Table 7. SRAM AC Characteristics—Read Operations

Number	Symbol	Parameter	Min	Max	Unit	Notes
R11	t_{BLZ}	R-UB#, R-LB# to Output in Low-Z	0	–	ns	1
R12	t_{BHZ}	R-UB#, R-LB# to Output in High-Z	0	25	ns	1

NOTES:

1. Sampled, not 100% tested.
2. At any given temperature and voltage condition, t_{HZ} (Max) is less than t_{LZ} (Max) for a given device and from device-to-device interconnection.
3. Timings of t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 4. SRAM Read Waveform

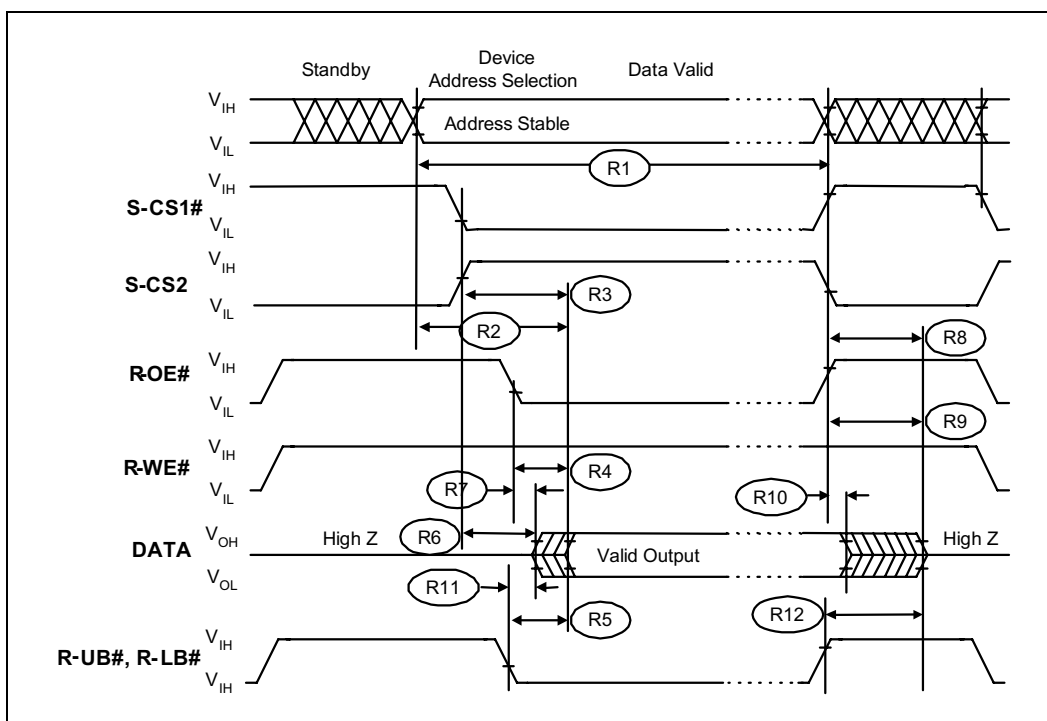


Table 8. SRAM AC Characteristics—Write Operations

Number	Symbol	Parameter	Min	Max	Unit	Notes
W1	t_{WC}	Write Cycle Time	70	–	ns	1
W2	t_{AS}	Address Setup to R-WE# (S-CS1#) and R-UB#,R-LB# Going Low	0	–	ns	3
W3	t_{WP}	R-WE# (S-CS1#) Pulse Width	55	–	ns	1
W4	t_{DW}	Data to Write Time Overlap	30	–	ns	
W5	t_{AW}	Address Setup to R-WE# (S-CS1#) Going High	60	–	ns	
W6	t_{CW}	S-CS1# (R-WE#) Setup to R-WE# (S-CS1#) Going High	60	–	ns	2
W7	t_{DH}	Data Hold from R-WE# (S-CS1#) High	0	–	ns	

Table 8. SRAM AC Characteristics—Write Operations

W8	t_{WR}	Write Recovery	0	–	ns	4
W9	t_{BW}	R-UB#, R-LB# Setup to R-WE# (S-CS1#) Going High	60	–	ns	

NOTES:

1. A write occurs during the S-CS1# and R-WE# asserted overlap (t_{WP}). The write begins with the latest transition of S-CS1# and R-WE# going low (R-UB# and/or R-LB# already asserted). The write ends at the earliest transition of S-CS1# or R-WE# going high.
2. t_{CW} is measured from S-CS1# going low to the end of a write.
3. t_{AS} is measured from address valid to the beginning of a write.
4. t_{WR} is measured from the end of a write to the address change; t_{WR} applied in case a write ends as S-CS1# or R-WE# going high.

Figure 5. SRAM Write Waveform

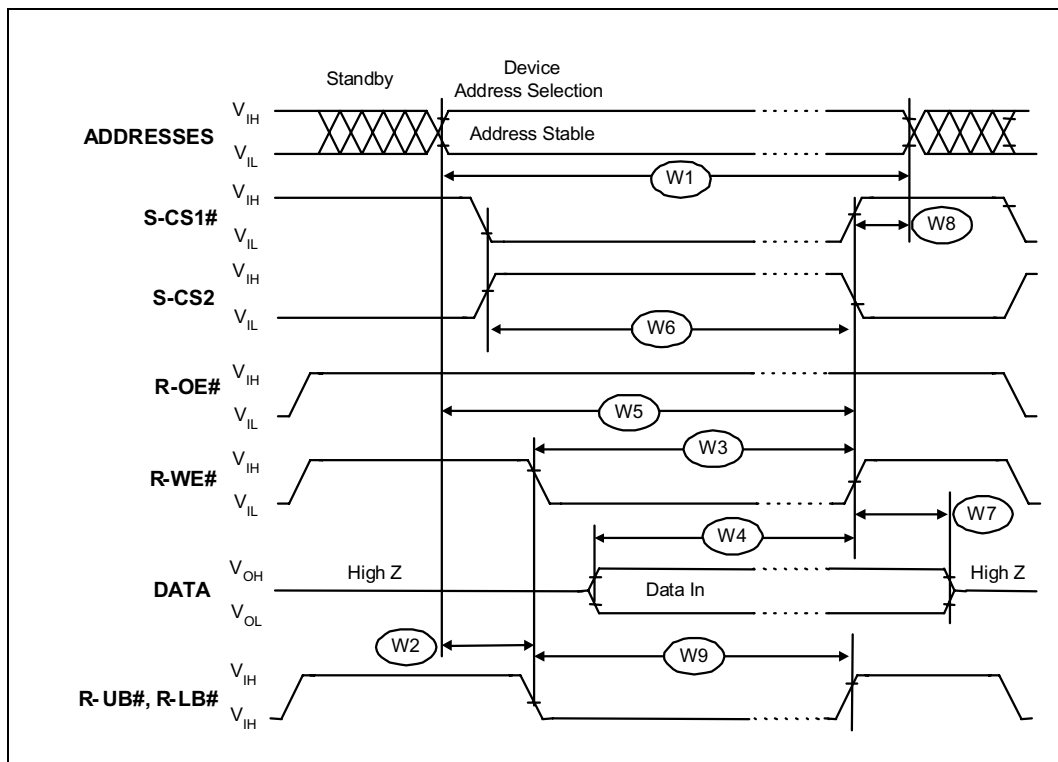


Figure 6. SRAM Data Retention Waveform (S-CS1# Controlled)

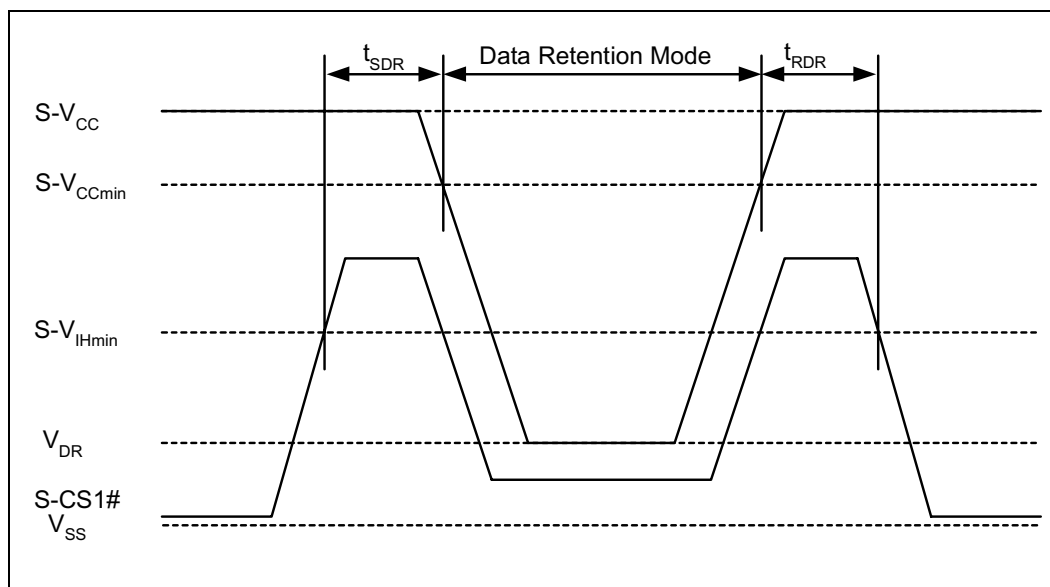
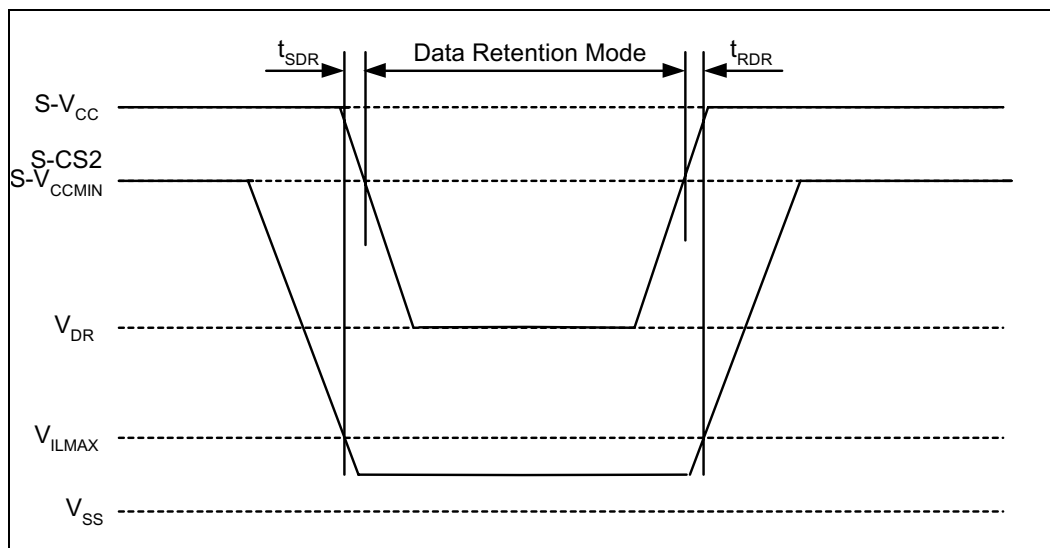


Figure 7. SRAM Data Retention Waveform (S-CS2 Controlled)



8.0 Power and Reset Specifications

For detailed information on this section, please reference the *Intel® Wireless Flash Memory (W18) Datasheet*.

9.0 Device Operation

Bus operations for the 38F1020W0YTQ0 and 38F1020W0YBQ0 devices involve the control of the flash and SRAM inputs. The flash memory is controlled via chip enable (CE#1) and output enable (OE#1).

Flash and SRAM bus operations are shown in Table 9, “Bus Operations” on page 19.

Refer to the discrete W18 datasheet for complete descriptions of flash modes and commands, and for command bus-cycle definitions and flowcharts that illustrate operational routines.

Table 9. Bus Operations

Device	Mode	RST#	CE#1	OE#1	WE#	VPP	WAIT	S-CS1#	S-CS2	R-OE#	R-WE#	R-UB#, R-LB#	D[15:0]	Notes
Flash	Read	H	L	L	H	X	Valid/ Driven	SRAM must be in High-Z					Flash D _{OUT}	1,2,3,5,6
	Write	H	L	H	L	V _{PP1} OR V _{PP2}	Driven						Flash D _{IN}	3,4,7
	Output Disable	H	L	H	H	X	Driven	Any SRAM mode allowed					Flash High-Z	5
	Standby	H	H	X	X	X	High-Z						Flash High-Z	5
	Reset	L	X	X	X	X	High-Z						Flash High-Z	5
SRAM	Read	Flash must be in High-Z					Note 2	L	H	L	H	L	SRAM D _{OUT}	1,4
	Write						Note 2	L	H	H	L	L	SRAM D _{IN}	4
	Output Disable						Note 2	L	H	H	H	X	SRAM High-Z	5
	Standby	Any Flash mode allowed					Note 2	H / X	X / L	X	X	X	SRAM High-Z	5,8
	Data Retention						Note 2	Same as SRAM standby					SRAM High-Z	9

NOTES:

1. For asynchronous read operation, both die may be simultaneously selected, but may not simultaneously drive the memory bus. For synchronous burst-mode reads, both die may be simultaneously selected.
2. WAIT is valid during synchronous Flash reads. WAIT is driven if CE#1 is asserted.
3. OE#1 and WE# should never be asserted simultaneously.
4. For SRAM, R-OE#1 and R-WE# should never be asserted simultaneously.
5. X can be V_{IL} or V_{IH} for inputs, V_{PP1}, V_{PP2} or V_{PPLK} for V_{PP}.
6. Flash CFI query and status register accesses use D[7:0] only, all other reads use D[15:0].
7. Refer to W18 datasheet for valid D_{IN} during Flash writes.
8. The SRAM is enabled and/or disabled with the logical function: S-CS1# OR S-CS2.
9. The SRAM can be placed into data retention mode by lowering S-VCC to the V_{DR} limit when in standby mode.

10.0 Flash Read Operations

For detailed information on this section, please reference the *Intel® Wireless Flash Memory (W18) Datasheet*.

11.0 Flash Program Operations

For detailed information on this section, please reference the *Intel® Wireless Flash Memory (W18) Datasheet*.

12.0 Flash Program and Erase Operations

For detailed information on this section, please reference the *Intel® Wireless Flash Memory (W18) Datasheet*.

13.0 Flash Security Modes

For detailed information on this section, please reference the *Intel® Wireless Flash Memory (W18) Datasheet*.

14.0 Flash Set Configuration Register

For detailed information on this section, please reference the *Intel® Wireless Flash Memory (W18) Datasheet*.

Appendix A Write State Machine

For detailed information on this section, please reference the *Intel® Wireless Flash Memory (W18) Datasheet*.

Appendix B Common Flash Interface

For detailed information on this section, please reference the *Intel® Wireless Flash Memory (W18) Datasheet*.

Appendix C Additional Information

Order Number	Document
290701	<i>Intel® Wireless Flash Memory (W18) Datasheet</i>
298289	<i>Intel® Wireless Flash Memory (W18) Specification Update</i>

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. For the most current information on Intel® Flash memory products, software and tools, visit our website at <http://developer.intel.com/design/flash>.

Appendix D Ordering Information

Figure 8. Ordering Information

